DESIGN OF LOW-POWER HIGH-GAIN OPERATIONAL AMPLIFIER FOR BIO-MEDICAL APPLICATIONS USING CLASS A AMPLIFIER

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ABSTRACT

The trend towards implementing systems with low supply voltages has created a challenging task in the design of VLSI analog circuits. The design of a low-power, high-gain and highly stable amplifier for bio-medical applications. Low power dissipation, high-gain are achieved. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails are preferable for low-voltage operation, especially if they do not increase the circuit complexity.

This comparator enhances the speed and performance for the low power supply voltage also. For this comparator we have to add the additional circuitry when compared to the conventional dynamic comparator. This design could be done through the TANNER EDA at 118nm CMOS technology.

INTRODUCTION

Realization of low-power high-gain system design is always a difficult goal as both requirements almost contradict each other. The increasing demand for portable equipment and its applicability in bio-medical applications has enhanced the importance of low power circuit design. The trend towards implementing systems with low supply voltages has created a challenging task in the design of VLSI analog circuits. The design of a low-power, high-gain and highly stable amplifier for bio-medical applications.

A BiCMOS class-AB op-amp that simultaneously reduces the slewing-time as well as the linear settling-time for light to moderate capacitive loads was presented. A unique class- AB input trans conductance stage that does not require the use of vertical-pnp transistors was presented and methods for Wide banding it were described. Simulation and measurement results confirmed the large slew-rate that this op-amp was capable of delivering. S. Sen and B. Leung, “A Class-AB high speed low power operational amplifier in BiCMOS technology,”

The design of low-noise tunable amplifiers employed in neural-recording sensor interface circuits were discussed and an in-depth analysis was presented. A three-stage amplifier comprising an LNA, a band-pass filter, and a VGA was demonstrated to minimize the area, reduce the total input-referred noise while preserving the linearity behavior of the circuit and driving a large input capacitance of the following ADC these two modes, benefiting from the linear behavior of a novel tunable. The mid-band gain and high cutoff frequency of the amplifier are tunable as...

R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications,'designed and tested a novel bioamplifier that uses a MOS-bipolar pseudo-resistor to amplify signals down to the mHz range while rejecting large dc offsets. We derive the theoretical noise-power tradeoff limit - the noise efficiency factor - for this amplifier and demonstrate that our VLSI implementation approaches that limit.

Y. Chih-Jen, C. Wen-Yaw, and C. M. Chen, "Micro-power low-offset instrumentation amplifier IC design for biomedical system applications," A micro-power low-offset CMOS integrated circuit for IA applications has been developed. Design techniques of offset cancellation and wide-swing cascode are used to improve the circuit performance. Circuit implementation for minimizing the dependence on process variation has also been described in detail. Experimental results manifest the amplifier has a high PSRR and a large operating range. The measured performance demonstrates that the IA is well suited to amplify the ECG signal in a biomedical system this amplifier design must reduce the supply voltage to 1.5 V for battery-operated applications, and further develop multichannel input data acquisition.

S. Ha, C. Kim, Y. M. Chi, A. Akinin, C. Maier, A. Ueno, and G. Cauwenberghs, “Integrated circuits and electrode interfaces for noninvasive physiological monitoring” focused on the integrated circuit techniques to improve the performance and expand the applications of noninvasive physiological monitoring instrumentation and discussed the challenges at the electrode–body interface. From these interface considerations, they developed system requirements for reliable signal acquisition in biopotential, electrode–tissue impedance, and spectrophotometric measurements. Some of the main techniques for implementing CMOS subthreshold integrated instrumentation amplifiers in a low-noise and power-efficient manner

**Existing System**

- A class-AB high speed low power operational amplifier
- Tunable amplifiers
- A low-power low-noise CMOS amplifier
  1) Cascading,
  2) Gain boosting and
  3) Applying positive feedback

**Drawbacks**

- Operation Speed and performance could be low.

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• Delay time is increased.
• High supply voltage.
• Transistors is high in final existing system

Proposed System

Higher gain and lower power consumption, this type of Op-Amp topology

The proposed AMPLIFIER works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 mhz and consumes low power.

Higher gain and lower power Op-Amp

A two-stage amplifier is designed, with the first stage being a simple differential stage and the second stage is a common source stage, having a compensation capacitor. In between the first and the second stage a current mirror topology is used that works as a sink for the current. The current mirror sums the differential current of first stage, feeding it to the second stage by the current mirror action. This topology provides highly stable system with a high gain and it also provides low power dissipation. Thus a low power high gain operational amplifier requires designing of sub-circuits. The various transistors and components need to be configured to accomplish the required specifications. Hence a proper design methodology is essential. These are detailed in this section.

Low-Power High-Gain Operational Amplifier (LPHG Op-Amp) Circuit

An Op-Amp, various difficulties occur with lower power supplies of the level of 2VT . The limit of low power supply voltage is related to the desired input common mode range. The LPHG Op-Amp is a current sink Op-Amp that provides high gain at lower supply voltage with very small power dissipation.

Equations (1) to (18) present the design relationships that are used in designing the overall proposed circuit. The dc gain of the Op-Amp \( AV \) (0) is given as

\[
Av (0) = GMI \times RI \times RII \times GMII
\]

where \( Av (0) \) is the dc gain of Op-Amp, \( GMI \) and \( GMII \) are the overall trans-conductance of the first and the second stages of Op-Amp respectively. \( RI \) and \( RII \) are the overall resistance of first and second stages of Op-Amp.
respectively. First step involves the computation of compensation capacitance ($C_c$). It is derived from angle equation of the Op-Amp transfer function. $C_c$ optimizes the phase margin of the system. This in turn makes system more stable. It is given as

$$C_c \geq 0.611CL$$  \hspace{1cm} (2)

where $CL$ is the load capacitor. Next step of design flow is to compute trans conductance of input transistors M1 and M2, in order to calculate their aspect ratio. The input stage amplifier trans-conductance is given as,

$$GM_1 = GB \times C_c$$  \hspace{1cm} (3)

where $GM_1$ the trans-conductance of input stage transistors. $GB$ is unity gain bandwidth. Bias current to generate biasing voltage is given by

$$I_{Bias} = C_c \times SR$$  \hspace{1cm} (4)

where $I_{Bias}$ is the bias current and $SR$ is the slew rate. MOSFET current ($I_d$) in saturation region is defined by.

$$I_d=k\times(V_g-V_t)^{1/2}$$  \hspace{1cm} (5)

Equation (5) is used to drive the relationship in terms of aspect ratio and the other known parameters values. It is defined in (6).

$$\frac{W}{L} = \frac{k'}{k}(\frac{W}{L})^{1/2}$$  \hspace{1cm} (6)

where $W/L$ is the trans-conductance of M1 and $k'$ is the process trans-conductance parameter of NMOS transistor. Using aspect ratio from (6), gate to source voltage ($V_{GS1}$) of transistor M1 is computed and given by (7).

$$V_{GS1} = \frac{2I_d}{k'W/L}$$  \hspace{1cm} (7)

For transistor M3 to be in saturation region of operation, the source to drain saturation voltage of M3 ($V_{SD3(SAT)}$) is computed using (8).

$$VICM(MAX) = VDD - V_{SD3(SAT)} + VTN$$  \hspace{1cm} (8)

Where $VICM(MAX)$ is the maximum input common-mode voltage, $VDD$ is supply voltage and $VTN$ represents threshold voltage of NMOS transistor. Subsequently, (9) is used to determine the aspect ratio of M3 and M4 transistors as

$$V_{max} = \frac{2I_d}{k'W/L}$$  \hspace{1cm} (9)

Equation (10) is used to calculate the saturation voltage across M5 ($V_{DS5(SAT)}$). It is given as,
\[ \text{VICM(MIN)} = V_{D55(SAT)} + V_{GS1} \quad (10) \]

Where \(\text{VICM(MIN)}\) is the minimum input common-mode voltage. Relationship to calculate aspect ratio of \(M5\) is obtained as

\[ V_{G11} = \sqrt{\frac{2I_{11}}{k_p^2 \cdot \left(\frac{W}{L}\right)}} \quad (11) \]

Similarly, (12) and (13) give the relationships to find the aspect ratio of \(M6\), \(M7\) and \(M8\), \(M9\) respectively.

\[ \frac{W_8}{L_8} = \frac{W_9}{L_9} = \frac{2 \cdot I_{11}}{k_p \cdot V^2_{DS11}} \quad (12) \]

\[ \frac{W_{12}}{L_{12}} = \frac{2 \cdot I_{11}}{k_p \cdot V^2_{DS11}} \quad (13) \]

\[ \frac{W_{11}}{L_{11}} = \frac{W_{12}}{L_{12}} = \frac{2 \cdot I_{11}}{k_p \cdot V^2_{DS11}} \quad (14) \]

\[ V_{GSS} = V_{DD} - 2V_{ON} \quad (15) \]

Schematic diagram

where, \(V_{ON}\) is the saturation voltage, which drive the transistors into the saturation region. This voltage is used to calculate the gate to source (\(V_{G58}\)) voltage of transistor \(M8\) that helps in calculating the size of transistor \(M8\). The aspect ratio of \(M13\) is computed using current through \(M13\) (\(I_{13}\)) , \(M12\) (\(I_{12}\)) and aspect ratio of \(M12\). It is given as,
The relationship between trans-conductance of transistors M1 and M14 is defined in (17). Using (17), aspect ratio of M14 is computed. These are given as,

\[
\frac{W_{14}}{L_{14}} = \left(\frac{I_{14}}{I_{12}}\right)\frac{W_{12}}{L_{12}}
\]

(16)

The advantage of the topology used in the present work is that it can be used at various low supply voltages with negligible variation in power consumption and gain. Owing to the higher gain and lower power consumption, this type of Op-Amp topology is at-most suited for biomedical applications and is analyzed in the present paper. The proposed schematic of low-power high-gain operational amplifier

**ADVANTAGES**

- Less power consumption.
- Less time consumption.
- Less delay.

**APPLICATIONS**

- MEDICAL
- Chip manufacturing

**SOFTWARE**

- TANNER EDA

**CONCLUSION**

Dical instruments has been presented in this paper. TheLPHG Op-Amp has a mid-band gain of 93dB with a bandwidth of 0.8 KHz while consuming 1.83mW of power. Power dissipation of the LPHG Op-Amp design is relatively high because high current flows through the output stage. However, compared to the specifications the design achieves lower power dissipation value. Also using this topology gives better input common mode (ICMR) voltage range. The ICMR is such that it does not show significant change with the variation of the supply voltage. Implementation of level shifter and implementation of common mode feedback circuitry shall be done which reduces the input noise and enhances the system performance. This type of Op-Amp can be used in bio-medical application because the bio-medical signal...
strength is low. In order to get the accurate results an amplifier with high gain and stability is required. The presented Op-Amp has this capability. Also this can be used in low dropout regulators where the low-power consumption is the main target, as the power consumed by the designed Op-Amp is very low with high-gain and high input common mode range.

RESULT

![Frequency response of LPHG Op-Amp](image)

**Fig. 3.** Frequency response of LPHG Op-Amp.